B1 D12 Cont'd

33 (new). A semiconductor device as claimed in claim 29, wherein the insulating layer has a moisture absorbable characteristic. --

REMARKS

The Examiner's Office Action of December 28, 2001 has been received and carefully reviewed. Claims 1, 3-5, 10, 11, 13-16, 19 and 20 are amended, and new claims 27-33 are added. Claims 21-26 are withdrawn from consideration. Thus, claims 1-20 and 27-33 are pending in this application. For at least the following reasons, it is submitted that this application is in condition for allowance.

Initially, it is noted that this Amendment increases the total number of claims pending in the application to twenty-seven (27) from twenty-six (26), thus, requiring a further excess claim fee of $ 18.00 for one excess claim. Please charge the necessary fee of $18.00 to our Deposit Account No. 50-0945.

In the Action, the examiner requires a new title of the invention because the title is not descriptive. Since the title has been amended to "SEMICONDUCTOR DEVICE HAVING WIRING PATTERNS and Dummy Patterns COVERED WITH INSULATING LAYER",

Applicant believes that the objection regarding the title is no longer applicable.

In the Action, the examiner requires a correction regarding the drawings (Figs. 8A-C) because Figs. 8A-C should be designated by a legend. Applicant agrees. In conformance with requirement of the examiner, the drawings (Figs. 8A-C) are amended by adding the term "PRIOR ART". Applicant believes that the objection regarding the drawings is no longer applicable.

In the Action, claim 5 is objected to because of the informalities. Since claim 5 has been amended by following the examiner's suggestion, Applicant believes that the objection regarding claim 5 is no longer applicable.

In the Action, claims 5-10, and 13 are rejected under 35 U. S. C. 112, second paragraph, as indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Since claims 5 and 13 have been amended by following the examiner's suggestion, Applicant believes that the rejection under 35 U. S. C. 112, second paragraph regarding claims 5-10 and 13 is no longer applicable.

In the Action, claims 1-6 and 8-15 are rejected under 35 U. S. C. 103(a) as being unpatentable over Yamaha et al. in view of Hosoda et al. The rejection is respectfully traversed.

The invention defined in claim 1 relates to a semiconductor device having wiring patterns covered with an insulating layer. The characteristics of the invention claimed in independent claim 1 are:

(a) a semiconductor substrate having a circuit area where an integrated circuit is formed and a peripheral area surrounding the circuit area,

(b) a dummy pattern (202a) formed in the peripheral area, and

(c) a second insulating layer (204) being **not** formed over the dummy pattern.

According to this structure, since the second insulating layer is not formed over the dummy pattern, which is formed in the peripheral area surrounding the circuit area, moisture cannot come into the circuit area through the second insulating layer so that it is possible to avoid corroding the wiring patterns formed in the circuit area.

However, Yamaha et al. do not disclose the characteristics described above. That is, Yamaha et al. simply disclose a dummy pattern 13, which planarizes a insulating layer 14 on which an upper layer wiring 15 is formed. In other words, the dummy pattern 13 is formed in a region where a lower layer wiring 12 is not formed closely, **not in the peripheral area surrounding the circuit area,** in order to planarize the surface of the insulating layer 14 because the thickness of the insulating layer 14 in the region where the lower layer wiring 12 is not formed closely is different from that in a region where the lower layer wiring 12 is formed closely. Thus, Yamaha et al. disclose that the dummy layer 13 is formed in the circuit area, not the peripheral area. As a result, Yamaha et al. cannot avoid coming moisture into the circuit area so that the lower layer wiring may be corroded by moisture. On the contrary, as described above, since a dummy layer 202a of the invention is formed in the peripheral area surrounding the circuit area and the second insulating layer 204 is not formed over the dummy layer 202a, moisture cannot come into the circuit area through the second insulating layer so that it is possible to avoid corroding the wiring patterns formed in the circuit area.

Further, the examiner asserts that Yamaha et al. disclose a dummy area (RB) in Fig. 5. Applicant disagrees. The area (RB) in Fig. 5 is a part of the circuit area but the peripheral area because an upper layer wiring 16, which is a part of an active circuit, is formed over the dummy layer 13. Thus, the area (RB) simply shows the region where the lower layer wiring 12 is not formed closely.

Moreover, Yamaha et al. disclose in the paragraph [0017] that there is the thin SOG insulating layer on the dummy pattern. This is quite different structure from that of the invention.

Hosoda et al. disclose a plurality of dummy patterns 14 or 14a to reduce wiring capacitance. According to Hosoda et al., the dummy patterns 14 or 14a are formed between the wirings 13 or between the wiring 13 and a guard pattern 15 in order to form cavities 17 between the wiring 13 and the dummy pattern 14 when the insulating layer 16 is formed. Therefore, in the disclosure of the Hosoda et al. reference, it is required to form the insulating layer 16 on the dummy layer. Therefore, Hosoda et al. cannot avoid coming moisture into the circuit area so that the wiring 13 may be corroded by moisture. On the contrary, according to the

invention, since the second insulating layer 204 is not formed over the dummy layer 202a, moisture cannot come into the circuit area through the second insulating layer so that it is possible to avoid corroding the wiring patterns formed in the circuit area.

The examiner asserts that Hosoda et al. teach that dummy pattern (14a) can be formed anywhere on a chip including surrounding the circuit pattern at the edge of the chip and that it would have been obvious to one having the skill in the art at the time of the invention to form the dummy pattern (13) of Yamaha et al. surrounding the circuit pattern (12s) as taught by Hosoda to improve the planarity of the insulating layer near the edge of the chip. Applicant disagree. First, as described above, the purpose for forming the dummy pattern 202a in the peripheral area surrounding the circuit area is not the improvement of the planarity of the insulating layer near the edge of the chip. The purpose for forming the dummy pattern in the peripheral area is to avoid coming moisture into the circuit area. Thus, the second insulating layer should not be formed on the dummy layer. Further, even if the dummy pattern 13 of Yamaha et al. surrounds the circuit pattern as taught by Hosoda, it is not possible to avoid coming moisture into the circuit area

because the insulating layer 14b of Yamaha et al. is formed on the dummy pattern 13.

Therefore, since Yamaha et al. and Hosoda et al. alone or in combination neither show nor suggest the characteristics (a) - (c) described above, which are defined in claim 1, claim 1 clearly is deemed to be clearly patentable over Yamaha et al. in view of Hosoda et al., and the rejection of claim 1 accordingly should be withdrawn. Further, claims 2-6 and 8-15 depend from claim 1 directly or indirectly so that the rejection of these claims also should be withdrawn. Moreover, regarding claim 5, the examiner asserts the dummy pattern can be formed on the first and second level of a three levels wiring because the device of Yamaha also includes multi-layered wiring. Applicant disagree. Yamaha et al. neither show nor suggest the second dummy pattern which is formed under the first dummy pattern. Applicant requires the detail explanation or necessity why the second dummy pattern shall be formed in the device of Yamaha.

Further, the examiner asserts that the expression "the width of the first (and third) dummy pattern is fixed by a concentration of solid content of the SOG (claims

3, 14 and 19); where a concentration of solid content of the SOG layer is around 5.2 wt% (claims 4, 10, 15 and 20); planarized by a thermal treatment (claim5) are taken to be a product by process limitation and is given no patentable weight. Since these claims have been amended, Applicant believes that the examiner's assertion is no longer applicable.

In the Action, claim 7 is rejected under 35 U. S. C. 103(a) as being unpatentable over Yamaha et al. and Hosoda et al. as applied to claim 5, and further in view of Hodate et al. The rejection is respectfully traversed.

First, claim 7 depends from clam 5, which depends from claim 1. First, as described above, Yamaha et al. and Hosoda et al. alone or in combination neither show nor suggest the characteristics (a) - (c) described above, which are defined in claim 1, specifically the characteristic that the second insulating layer is not formed above the dummy layer. Next, Hodate et al. simply disclose a dummy pattern 3, which is formed in order to raise a periphery of a bonding pad 14, which is formed in the circuit area, not in the peripheral area. Further, Hodate et al. do not disclose the wiring pattern and the second insulating layer formed above the wiring pattern.

Therefore, since Yahama et al., Hosoda et al. and Hodate et al. do not disclose neither the dummy pattern formed in the peripheral area and the second insulating layer being not formed above the wiring pattern nor the characteristics (a)-(c) described above, claim 7 clearly is deemed to be clearly patentable over Yamaha et al. and Hosoda et al. as applied to claim 5, and further in view of Hodate et al., and the rejection of claim 7 accordingly should be withdrawn.

In the Action, claims 16 - 20 are rejected under 35 U. S. C. 103(a) as being unpatentable over Yamaha et al. and Hosoda et al. as applied to claim 1, and further in view of Yang et al. The rejection is respectfully traversed.

First, claims 16 - 20 depend from claim 1 directly or indirectly. First, as described above, Yamaha et al. and Hosoda et al. alone or in combination neither show nor suggest the characteristics (a) - (c) described above, which are defined in claim 1, specifically the characteristic that the second insulating layer is not formed above the dummy layer. Next, Yang et al. simply disclose that a dummy metal 34 is formed between metal lines 30, 31 for the planarization. Therefore, not only the

dummy layer is formed in the circuit area, but also an insulating layer 36 is formed above the dummy layer. Therefore, in the device of Yang, it is impossible to avoid coming moisture into the circuit area. Therefore, since Yahama et al., Hosoda et al. and Yang et al. do not disclose neither the dummy pattern formed in the peripheral area and the second insulating layer not being formed above the wiring pattern nor the characteristics (a)-(c) described above, claim 16-20 clearly is deemed to be clearly patentable over Yamaha et al. and Hosoda et al. as applied to claim 1, and further in view of Yang et al., and the rejection of claim 16-20 accordingly should be withdrawn.

At page 8, lines 16-18 in the Action, the examiner asserts that with respect to "the first insulating layer(which has been amended to the second insulating layer) being not formed on the fourth dummy layer", the embodiment of Fig. 5 of Yamaha that the insulating layer (14b) is only formed over the circuit pattern not on the first dummy pattern (34). This is not true. As described above, Yamaha et al. disclose in the paragraph [0017] that there is the thin SOG insulating layer on the dummy pattern.

In view of the foregoing, the application is deemed to be in condition for allowance and such is earnestly solicited. Should any further fee be needed, please charge it to our Account No. 50-0945 and notify us accordingly.

Attached hereto is a marked-up version of the changes made to the drawings, title and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

Respectfully submitted,

Junichi MIMURA
(Registration No.40,351)
Oki America, Inc.
1101 14th Street, N.W., Suite 555
Washington, D.C. 20005
Telephone: (202) 452-6190
Telefax: (202) 452-6148
Customer No.: 26071

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the drawings:

In Figs. 8A – 8C, the term "PRIOR ART" has been added.

In the title of the invention

The title of the invention has been amended as follows:

SEMICONDUCTOR DEVICE HAVING WIRING PATTERNS COVERED WITH INSULATING LAYER

In the claims:

Claims 1, 3-5, 10, 11, 13-16, 19 and 20 have been amended as follows, and new claims 27-33 have been added.

1 (amended). A semiconductor device, comprising:

a semiconductor substrate having ~~a grid line area and a chip area, the chip area having~~ a circuit area where an integrated circuit is formed and a peripheral ~~dummy~~ area surrounding the circuit area;

wiring ~~circuit~~ patterns formed on the substrate in the circuit area;

a first dummy pattern which is formed of the same material as the wiring ~~circuit~~ pattern, formed in the peripheral ~~dummy~~ area, the dummy pattern encompassing the circuit area;

a first insulating layer formed on the circuit area and the peripheral area ~~an entire surface~~ of the semiconductor substrate;

a second insulating layer formed ~~only~~ on the first insulating layer which is formed on the semiconductor substrate ~~and on the circuit patterns~~ , wherein the second insulating layer is not formed over the first dummy pattern; and

a third insulating layer formed on the exposed first insulating layer and the second insulating layer.

3 (amended). A semiconductor device as claimed in claim 2, wherein the first dummy pattern has a width, which ~~of the first dummy pattern~~ is fixed by a concentration of solid content of the SOG layer.

4 (amended). A semiconductor device as claimed in claim 1, wherein the first dummy pattern has a width, which ~~of the first dummy pattern~~ is designed for less than 1 μm where a concentration of solid content of the SOG layer is around 5.2 wt%.

5 (amended). A semiconductor device as claimed in claim 1, further comprising:~~,~~

a second dummy pattern ~~patter~~ formed under the first dummy pattern; and

a fourth insulating layer formed directly on the substrate and on the second dummy pattern ~~layer~~, the fourth insulating layer including a thermally planarized surface. ~~having characteristics that its surface is planarized by a thermal treatment,~~

whereby, the first dummy pattern is formed on the fourth insulating layer which is formed on the second ~~first~~ dummy pattern ~~layer~~, and the wiring ~~circuit~~ patterns are formed on the fourth insulating layer.

10 (amended). A semiconductor device as claimed in claim 6, wherein each of the first and second dummy patterns has a width, which is ~~the widths of the first and second dummy patterns are~~ designed for less than 1 μm where a concentration of solid content of the SOG layer is around 5.2 wt%.

11 (amended). A semiconductor device as claimed in claim 1, further comprising:~~,~~

a third dummy pattern formed in the peripheral area between the first dummy pattern and the wiring patterns ~~circuit area~~, the first insulating layer being

not formed on the third dummy pattern.

13 (amended). A semiconductor device as claimed in claim 11, wherein the distance between the first dummy pattern and the third ~~second~~ dummy pattern is designed for over 0.9 μm.

14 (amended). A semiconductor device as claimed in claim 12, wherein each of the first and third dummy layer has a width, which is ~~the widths of the first and third dummy patterns are~~ fixed by a concentration of solid content of the SOG layer.

15 (amended). A semiconductor device as claimed in claim 12, wherein each of the first and third dummy layer has a width, which is ~~widths of the first and third dummy patterns are~~ designed for less than 1 μm where a concentration of solid content of the SOG layer is around 5.2 wt%.

16 (amended). A semiconductor device as claimed in claim 1, further comprising:~~,~~

a bonding pad formed on the semiconductor substrate in the circuit area; and

a fourth dummy pattern surrounding the bonding pad, the second ~~first~~ insulating layer being not formed on the fourth dummy layer.

19 (amended). A semiconductor device as claimed in claim 17, wherein each of the first and fourth dummy layer has a width, which is ~~the widths of the first and fourth dummy patterns are~~ fixed by a concentration of solid content of the SOG layer.

20 (amended). A semiconductor device as claimed in claim 17 ~~117~~, wherein each of the first and fourth dummy layer has a width, which is ~~widths of the first and fourth dummy patterns are~~ designed for less than 1 μm where a concentration of solid content of the SOG layer is around 5.2 wt%.